

### Safe Harbor



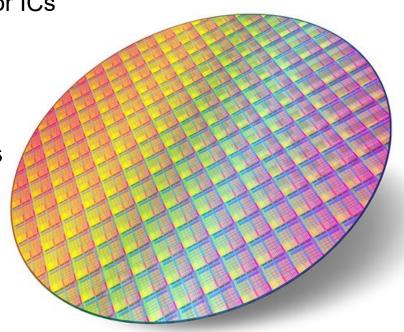
This presentation contains forward-looking statements concerning Atomera Incorporated (""Atomera," the "Company," "we," "us," and "our"). The words "believe," "may," "will," "potentially," "estimate," "continue," "anticipate," "intend," "could," "would," "project," "plan," "expect" and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section "Risk Factors" included in our Annual Report on Form 10-K filed with the SEC on February 15, 2022. In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

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### **Investment Overview**



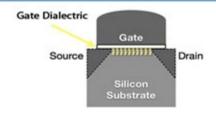
- ▶ Mears Silicon Technology (MST®) is a thin film used to enhance semiconductors
  - Results in higher performance, lower power, and lower costs for ICs
- Capital-light IP and technology licensing business
- Engaged with 50% of world's top semiconductor makers
- ► Licenses with five companies including two JDA
- Strong team to commercialize technology



### MST Technology



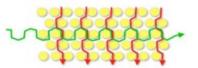
#### STANDARD SILICON TRANSISTOR



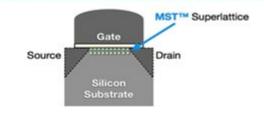
Standard Silicon Atomic Structure



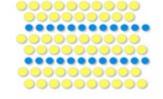
LIMITED Horizontal Current Flow + EXCESSIVE Vertical Leakage



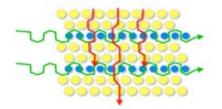
#### MST SILICON TRANSISTOR



MST™ Silicon Atomic Structure



INCREASED Horizontal Current Flow + REDUCED Vertical Leakage



#### **Potential Benefits**

#### ► Improved Efficiency

- Higher transistor performance
- Lower power consumption
- Better reliability

#### **▶** Lower cost

- Reduced die size
- Improved yield
- Higher throughput

► Same benefits as a node shrink

### Target Customers & Partners



#### **Integrated Device Manufacturers**

























#### **Foundry**

















#### **Fabless**

















**Tool Suppliers (Partners)** 







SYNOPSYS°

## Customer Pipeline



		Customer Wafer Manufacturing									
		Ato	omera MST® Deposition	Customer MST® Deposition							
Phase	1. Planning	2. Setup	3. Integration	<b>4</b> . Installation	<b>5</b> . Qualification	6. Production					

#### **Number of Customer Engagements**

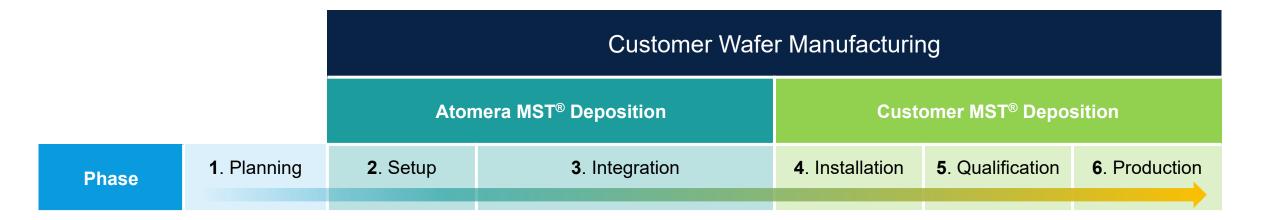


- 20 customers, 26 engagements
- Working with 50% of the world's top semiconductor makers\*

- 10 of the top 20 (IC Insights, McClean Report 2022)
- ^ End of year engagement count

### Customer Engagement & Revenue Model





Engineering Service Fees

- MST deposition on customer wafers
- Integration consulting

License Fees

- Integration licenses
- Manufacturing licenses
- Distribution licenses

**Joint Development Agreements** 

**Royalties** 

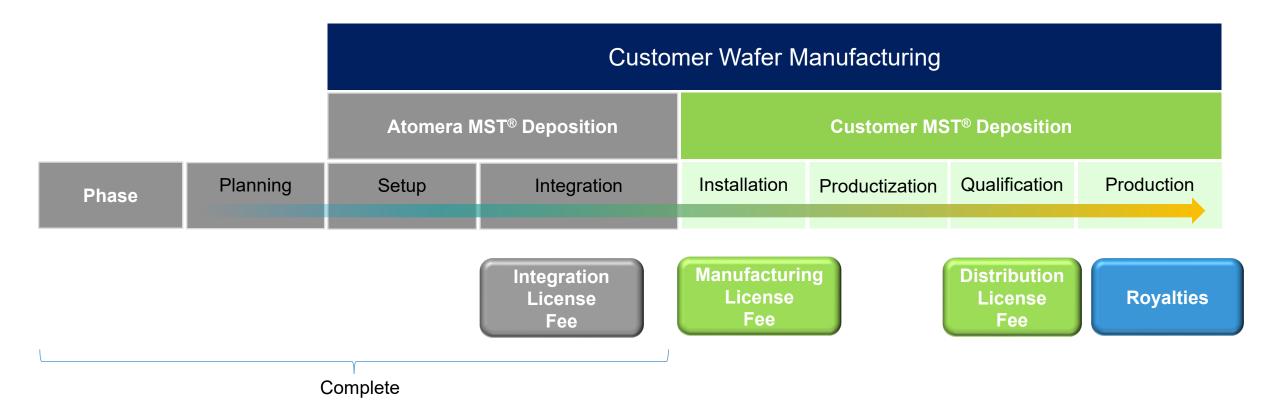




Atomera Incorporated 8

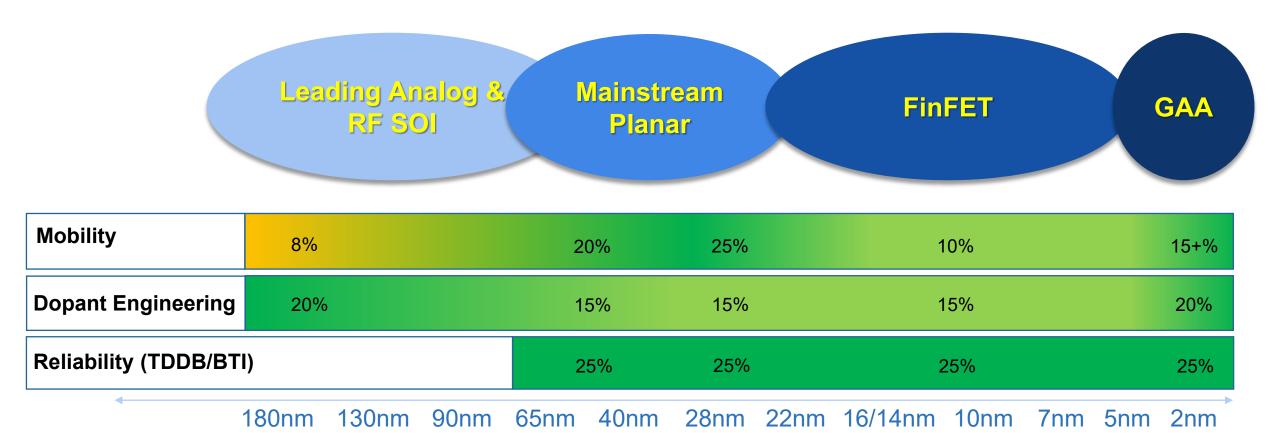
### ST Path to Production





### MST Key Benefits Across Nodes





These Benefits are ADDITIVE & COMPLEMENTARY to other enhancement technologies

# MST technology focus areas

atomera

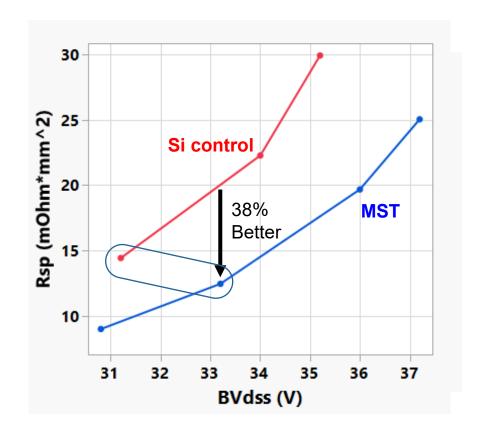
**MST-SP MST** for **Advanced** Nodes



### MST-SPX targeting power devices



- ► Targets higher voltage (5-40V) product area
- Strong customer demand for solutions
- ► MST brings significant improvement
  - Early results showing gains in many areas
  - Allows manufacturers to shrink designs, cut product costs
- ► Early stages of customer rollout

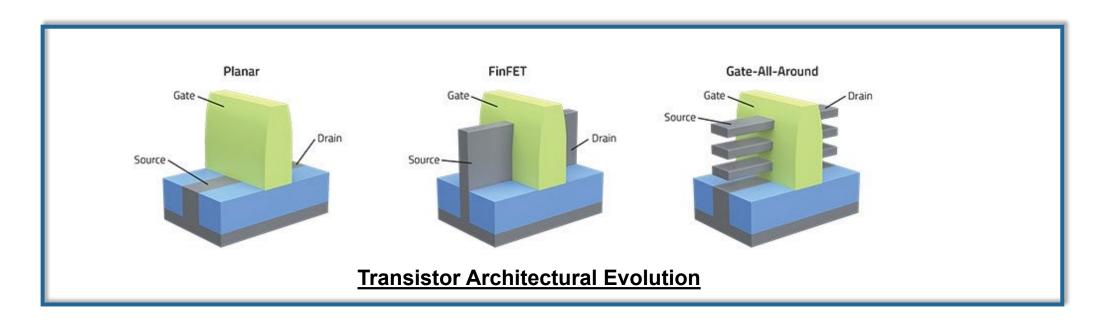


 $L_{DEVICE} = 1.84um$ 

### MST: Solving GAA Transistor Challenges



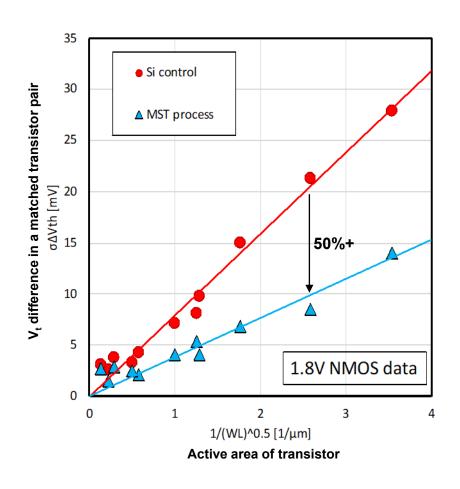
- ► Blocks source/drain dopant diffusion
- Provides enhanced punch-through stop layer between source and drain
- ► Lowers contact resistance
- Reduces HKMG stack height
- ► Improves carrier mobility, gate leakage



### Variability reduction with MST



- ▶ High variability between transistors is a significant issue
  - A big driver of variability is Random Dopant Fluctuation (RDF)
  - Some transistors are designed larger to account for variability
  - This increases costs and limits the minimum achievable voltage and power
- Advanced GAA transistor need solutions for RDF
- DRAM sense-amp variability is a major design constraint
  - Sense-amp margin defines refresh interval and resulting power
  - Improving variability allows smaller sense-amp and reduced power
- MST can minimize RDF and lower variability, critical in advanced nodes and memories



### Royalty Opportunity



- ► ~410 wafer fabs operating worldwide
- ► Adoption of MST in one fab can make Atomera profitable from royalties alone
  - 2023 non-GAAP OPEX guidance is \$16.25M \$16.75M

Example 1   Worldwide Average Fab								
Monthly Fab Capacity <sup>1</sup> (wafers/month)	46,240							
Industry average wafer ASP - 2018	\$1,365							
Annual Revenue Potential <sup>2</sup>	\$15.1M							
Annual Revenue at 50% of ramp <sup>2</sup>	\$7.6M							

Example 2   Leading Foundry, 28nm Fab								
Monthly Fab Capacity (wafers/month)	80,000							
Industry average 28nm wafer ASP	\$3,300							
Annual Revenue Potential <sup>2</sup>	\$63M							
Annual Revenue at 50% of ramp <sup>2</sup>	\$31.7M							

<sup>1.</sup> Represents wafers starts per month (200mm equiv) – 227.5M starts in 410 fabs

Source: IC Insights Global Wafer Capacity 2021-2025 report, McClean Report 2021, 2022

<sup>2.</sup> Assumes 2% royalty rate

### MST Customer Business Opportunity



#### ► Foundry economics

Wafer			GM\$		MST		Wafer		
	Price	GM%	Increase		Royalty		Cost		
28nm HP wafer	\$ 3,300	45%	\$	-	\$	-	\$	1,815	
28nm HP+ wafer	\$ 3,450	45%	\$	68	\$	-			5% higher price for +15% performance boost
28nm HP wafer with MST	\$ 3,600	47.0%	\$ 2	208	\$	72	\$	1,907	30% performance boost=10% higher price (+ \$20 MST cost)
28nm HP wafer with MST	\$ 3,713	48.6%	\$ 3	318	\$	74	\$	1,909	25% die shrink=12.5% price increase (+ \$20 MST cost)

- Gross margin increases by \$200-\$300 per wafer after foundry pays Atomera royalties
- ► Fabless semiconductor economics

	Chip sales/ wafer	GM%	GM\$	Product ASP	Die/wafer	
28nm HP wafer	\$ 9,233	50%	\$ -	\$ 4.86	2,235	Baseline business for 30mm <sup>2</sup> chip
28nm HP wafer with MST	\$ 12,398	59%	\$ 3,165	\$ 4.86	3,001	Improved financials with 25% size reduction

- Sales and profit both increase by over \$3000 per wafer for fabless manufacturer
- ► Everyone in the value chain benefits from MST technology





Income Statement	Three Months Ended									
(\$ in thousands, except per-share data)	J	une 30, 2023	N	March 31, 2023	June 30, 2022					
REVENUE			\$	-	\$	-				
Gross Profit				-		-				
OPERATING EXPENSES										
Research & Development		3,192		3,036		2,433				
General and Administration		1,775		1,742		1,667				
Selling and Marketing		393		389		347				
TOTAL OPERATING EXPENSES		5,360		5,167		4,447				
OPERATING LOSS		(5,360)		(5,167)		(4,447)				
Other Income (Expense)		208		148		(34)				
NET LOSS	\$	(5,152)	\$	(5,019)	\$	(4,481)				
Net Loss Per Share	\$	(0.21)	\$	(0.21)	\$	(0.20)				
Weighted average shares outstanding		24,677		23,660		22,936				
ADJUSTED EBITDA (NON-GAAP)	\$	(4,310)	\$	(4,220)	\$	(3,569)				
ADJUSTED EBITDA PER SHARE	\$	(0.17)	\$	(0.18)	\$	(0.16)				
Balance Sheet Information										
Cash, equivalents & ST investments	\$	23,835	\$	17,052	\$	21,838				
Debt				-		-				

### Summary



- ► High margin, recurring revenue financial model
- Strong technology, patent position, and balance sheet
- Traction with many top industry players and growing licensee base
- Ramping commercial license revenues

